

# 1.35V DDR3L SDRAM

**MT41K1G4 – 128 Meg x 4 x 8 banks**

**MT41K512M8 – 64 Meg x 8 x 8 banks**

**MT41K256M16 – 32 Meg x 16 x 8 banks**

## Description

DDR3L SDRAM (1.35V) is a low voltage version of the DDR3 SDRAM (1.5V).

### Features

- $V_{DD} = V_{DDQ} = 1.35V$  (1.283–1.45V)
- Backward compatible to  $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$ 
  - Supports DDR3L devices to be backward compatible in 1.5V applications
- Differential bidirectional data strobe
- $8n$ -bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode

- $T_C$  of 0°C to +95°C
  - 64ms, 8192-cycle refresh at 0°C to +85°C
  - 32ms at +85°C to +95°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

### Options

- Configuration
  - 1 Gig x 4
  - 512 Meg x 8
  - 256 Meg x 16
- FBGA package (Pb-free) – x4, x8
  - 78-ball (10.5mm x 12mm) Rev. D
  - 78-ball (9mm x 10.5mm) Rev. E, J
- FBGA package (Pb-free) – x16
  - 96-ball (10mm x 14mm) Rev. D
  - 96-ball (9mm x 14mm) Rev. E
- Timing – cycle time
  - 1.071ns @ CL = 13 (DDR3-1866)
  - 1.25ns @ CL = 11 (DDR3-1600)
  - 1.5ns @ CL = 9 (DDR3-1333)
  - 1.87ns @ CL = 7 (DDR3-1066)
- Operating temperature
  - Commercial (0°C ≤  $T_C$  ≤ +95°C)
  - Industrial (–40°C ≤  $T_C$  ≤ +95°C)
- Revision

### Marking

1G4  
512M8  
256M16

RA  
RH

RE  
HA

-107  
-125  
-15E  
-187E

None  
IT  
:D/:E/:J

**Table 1: Key Timing Parameters**

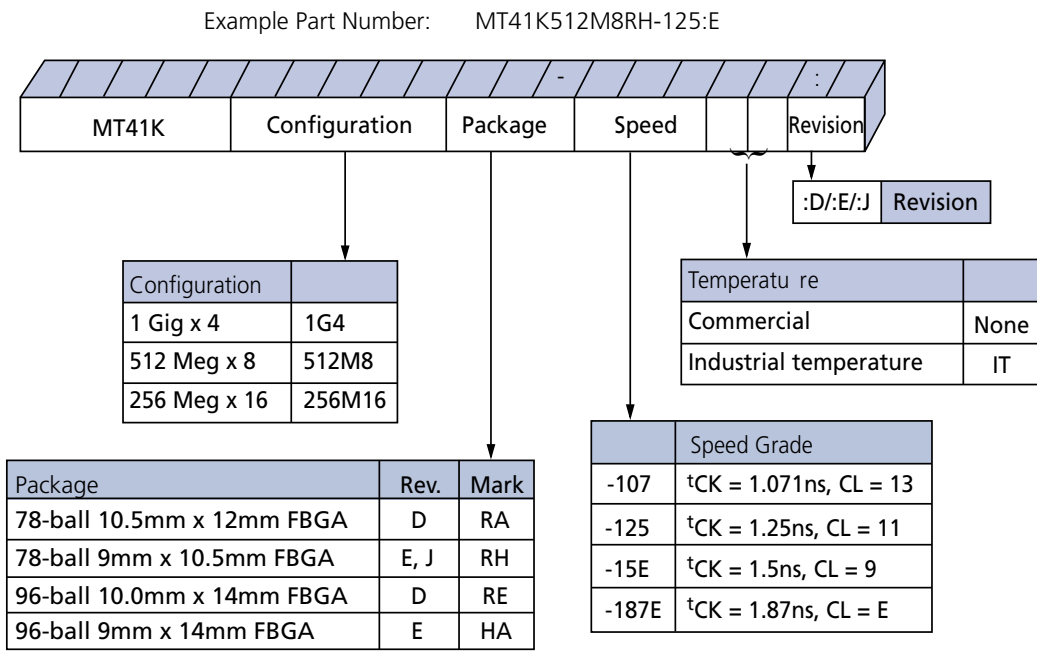
Speed Grade	Data Rate (MT/s)	Target $t_{RCD}$ - $t_{RP}$ -CL	$t_{RCD}$ (ns)	$t_{RP}$ (ns)	CL (ns)
-107 <sup>1, 2, 3</sup>	1866	13-13-13	13.91	13.91	13.91
-125 <sup>1, 2</sup>	1600	11-11-11	13.75	13.75	13.75
-15E <sup>1</sup>	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

- Notes: 1. Backward compatible to 1066, CL = 7 (-187E).  
 2. Backward compatible to 1333, CL = 9 (-15E).  
 3. Backward compatible to 1600, CL = 11 (-107).

**Table 2: Addressing**

Parameter	1 Gig x 4	512 Meg x 8	256 Meg x 16
Configuration	128 Meg x 4 x 8 banks	64 Meg x 8 x 8 banks	32 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row address	64K (A[15:0])	64K (A[15:0])	32K (A[14:0])
Bank address	8 (BA[2:0])	8 (BA[2:0])	8 (BA[2:0])
Column address	2K (A[11, 9:0])	1K (A[9:0])	1K (A[9:0])
Page size	1KB	1KB	2KB

**Figure 1: DDR3L Part Numbers**



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on <http://www.micron.com> for available offerings.

## FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at [www.micron.com/decoder](http://www.micron.com/decoder).

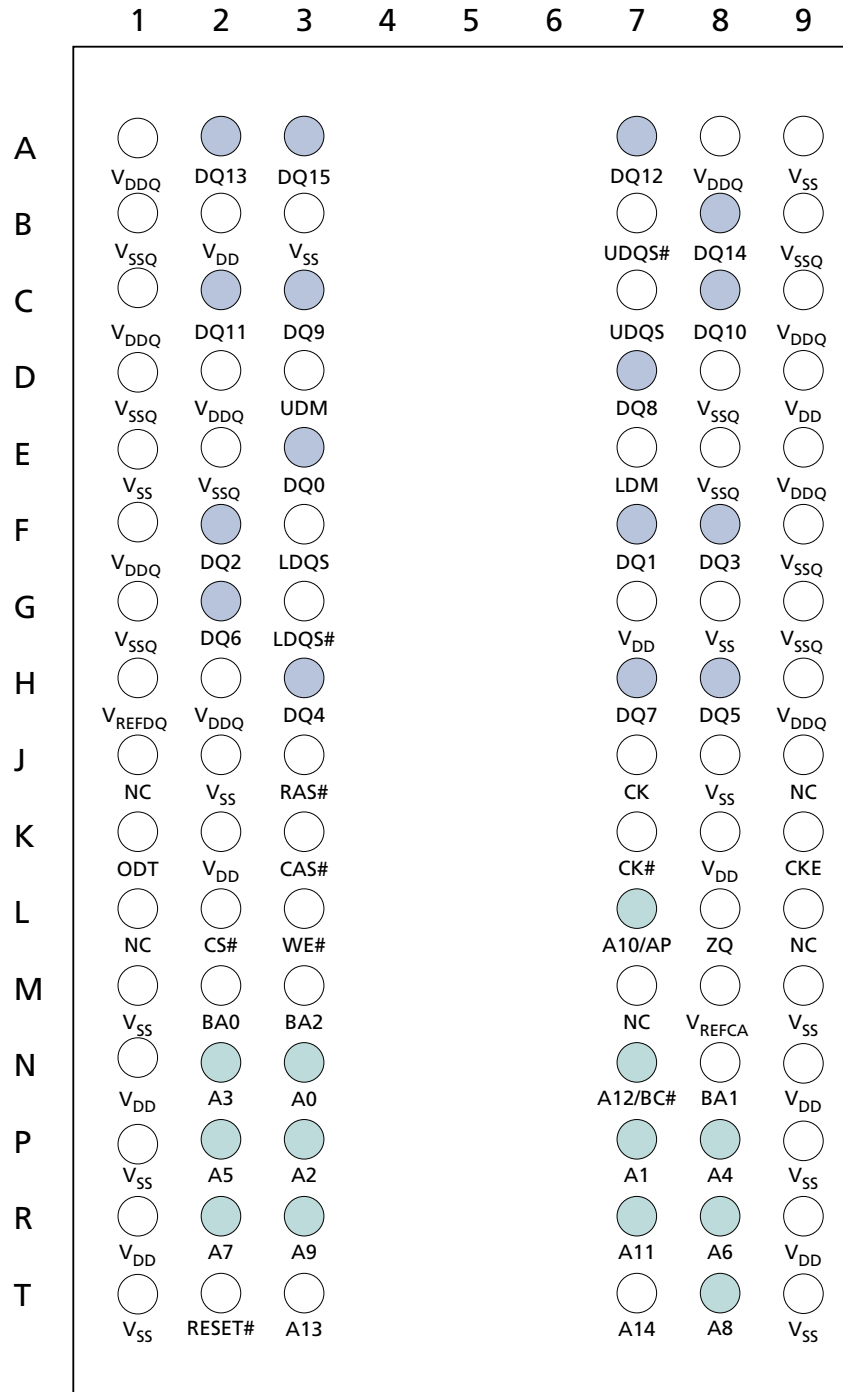
## Ball Assignments and Descriptions

**Figure 2: 78-Ball FBGA – x4, x8 (Top View)**

	1	2	3	4	5	6	7	8	9
A	V <sub>SS</sub>	V <sub>DD</sub>	NC				NF, NF/TDQS#	V <sub>SS</sub>	V <sub>DD</sub>
B	V <sub>SS</sub>	V <sub>SSQ</sub>	DQ0				DM, DM/TDQS	V <sub>SSQ</sub>	V <sub>DDQ</sub>
C	V <sub>DDQ</sub>	DQ2	DQ5				DQ1	DQ3	V <sub>SSQ</sub>
D	V <sub>SSQ</sub>	NF, DQ6	DQ5#				V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SSQ</sub>
E	V <sub>REFDQ</sub>	V <sub>DDQ</sub>	NF, DQ4				NF, DQ7	NF, DQ5	V <sub>DDQ</sub>
F	NC	V <sub>SS</sub>	RAS#				CK	V <sub>SS</sub>	NC
G	ODT	V <sub>DD</sub>	CAS#				CK#	V <sub>DD</sub>	CKE
H	NC	CS#	WE#				A10/AP	ZQ	NC
J	V <sub>SS</sub>	BA0	BA2				A15	V <sub>REFCA</sub>	V <sub>SS</sub>
K	V <sub>DD</sub>	A3	A0				A12/BC#	BA1	V <sub>DD</sub>
L	V <sub>SS</sub>	A5	A2				A1	A4	V <sub>SS</sub>
M	V <sub>DD</sub>	A7	A9				A11	A6	V <sub>DD</sub>
N	V <sub>SS</sub>	RESET#	A13				A14	A8	V <sub>SS</sub>

- Notes:
- Ball descriptions listed in Table 3 (page 5) are listed as “x4, x8” if unique; otherwise, x4 and x8 are the same.
  - A comma separates the configuration; a slash defines a selectable function. Example D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3).

**Figure 3: 96-Ball FBGA – x16 (Top View)**



Note: 1. A slash defines a selectable function.

**Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions**

Symbol	Type	Description
[15:13], A12/BC#, A11, A10/AP, A[9:0]	Input	<b>Address inputs:</b> Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to $V_{REFCA}$ . A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See Truth Table - Command in the DDR3 SDRAM data sheet.
BA[2:0]	Input	<b>Bank address inputs:</b> BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to $V_{REFCA}$ .
CK, CK#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	<b>Clock enable:</b> CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to $V_{REFCA}$ .
CS#	Input	<b>Chip select:</b> CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to $V_{REFCA}$ .
DM	Input	<b>Input data mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to $V_{REFDQ}$ . DM has an optional use as TDQS on the x8.
ODT	Input	<b>On-die termination:</b> ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to $V_{REFCA}$ .
RAS#, CAS#, WE#	Input	<b>Command inputs:</b> RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to $V_{REFCA}$ .
RESET#	Input	<b>Reset:</b> RESET# is an active LOW CMOS input referenced to $V_{SS}$ . The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times V_{DD}$ and DC LOW $\leq 0.2 \times V_{DDQ}$ . RESET# assertion and desertion are asynchronous.

**Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions (Continued)**

Symbol	Type	Description
DQ[3:0]	I/O	<b>Data input/output:</b> Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to $V_{REFDQ}$ .
DQ[7:0]	I/O	<b>Data input/output:</b> Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to $V_{REFDQ}$ .
DQS, DQS#	I/O	<b>Data strobe:</b> Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	Output	<b>Termination data strobe:</b> Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
$V_{DD}$	Supply	<b>Power supply:</b> 1.35V, 1.283–1.45V operational; compatible to 1.5V operation.
$V_{DDQ}$	Supply	<b>DQ power supply:</b> 1.35V, 1.283–1.45V operational; compatible to 1.5V operation.
$V_{REFCA}$	Supply	<b>Reference voltage for control, command, and address:</b> $V_{REFCA}$ must be maintained at all times (including self refresh) for proper device operation.
$V_{REFDQ}$	Supply	<b>Reference voltage for data:</b> $V_{REFDQ}$ must be maintained at all times (excluding self refresh) for proper device operation.
$V_{SS}$	Supply	Ground.
$V_{SSQ}$	Supply	<b>DQ ground:</b> Isolated on the device for improved noise immunity.
ZQ	Reference	<b>External reference ball for output drive calibration:</b> This ball is tied to an external 240Ω resistor (RZQ), which is tied to $V_{SSQ}$ .
NC	–	<b>No connect:</b> These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	<b>No function:</b> When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

**Table 4: 96-Ball FBGA – x16 Ball Descriptions**

Symbol	Type	Description
[14:13], A12/BC#, A11, A10/AP, A[9:0]	Input	<b>Address inputs:</b> Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to $V_{\text{REFCA}}$ . A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See Truth Table - Command in the DDR3 SDRAM data sheet.
BA[2:0]	Input	<b>Bank address inputs:</b> BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to $V_{\text{REFCA}}$ .
CK, CK#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	<b>Clock enable:</b> CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to $V_{\text{REFCA}}$ .
CS#	Input	<b>Chip select:</b> CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to $V_{\text{REFCA}}$ .
LDM	Input	<b>Input data mask:</b> LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to $V_{\text{REFDQ}}$ .
ODT	Input	<b>On-die termination:</b> ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16; DQ0[7:0], DQS, DQS#, DM/TDQS, and NF/TDQS# (when TDQS is enabled) for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to $V_{\text{REFCA}}$ .
RAS#, CAS#, WE#	Input	<b>Command inputs:</b> RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to $V_{\text{REFCA}}$ .

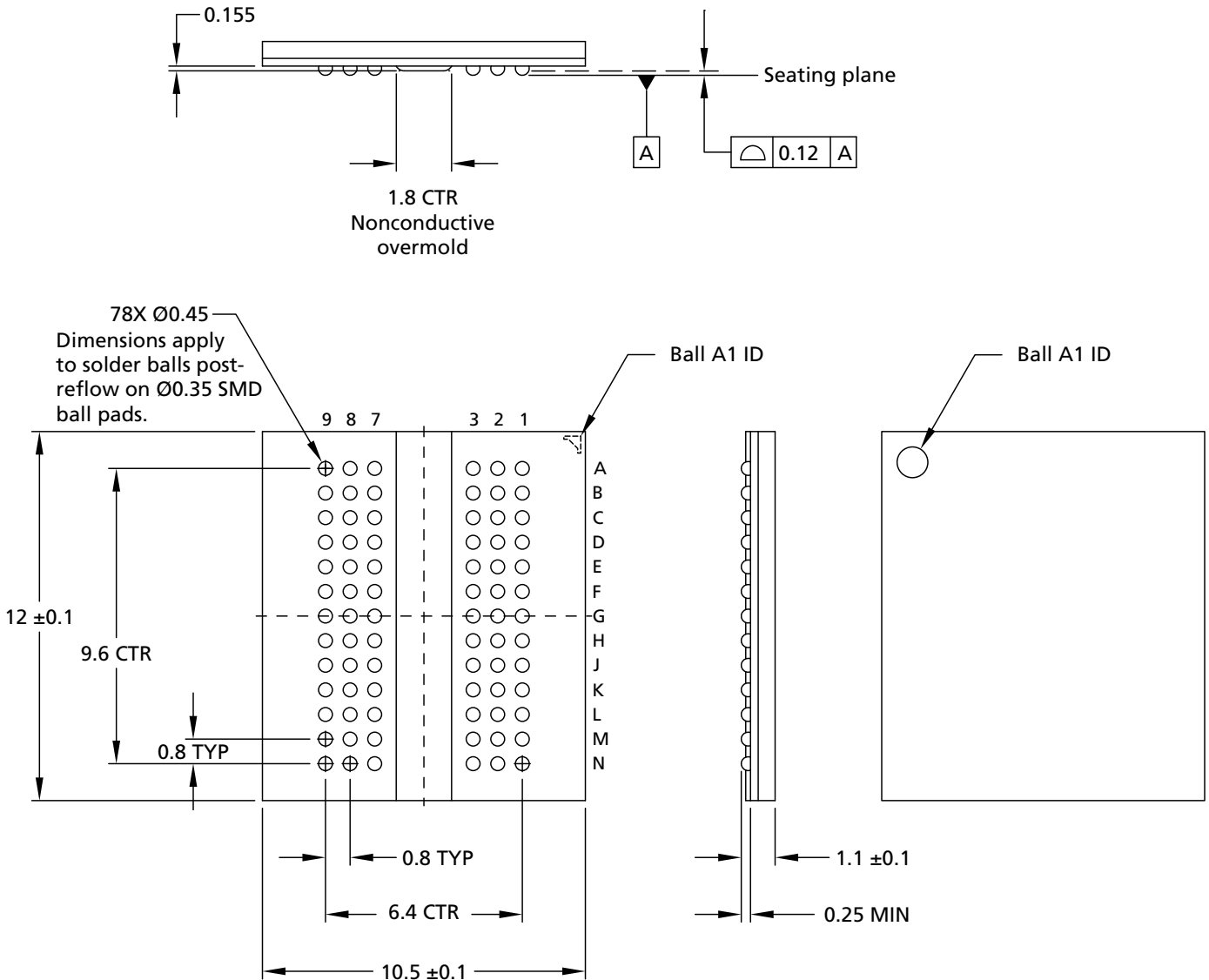
**Table 4: 96-Ball FBGA – x16 Ball Descriptions (Continued)**

Symbol	Type	Description
RESET#	Input	<b>Reset:</b> RESET# is an active LOW CMOS input referenced to $V_{SS}$ . The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times V_{DD}$ and DC LOW $\leq 0.2 \times V_{DDQ}$ . RESET# assertion and desertion are asynchronous.
UDM	Input	<b>Input data mask:</b> UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to $V_{REFDQ}$ .
DQ[7:0]	I/O	<b>Data input/output:</b> Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to $V_{REFDQ}$ .
DQ[15:8]	I/O	<b>Data input/output:</b> Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to $V_{REFDQ}$ .
LDQS, LDQS#	I/O	<b>Lower byte data strobe:</b> Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
UDQS, UDQS#	I/O	<b>Upper byte data strobe:</b> Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data.
$V_{DD}$	Supply	<b>Power supply:</b> 1.35V, 1.283–1.45V operational; compatible to 1.5V operation.
$V_{DDQ}$	Supply	<b>DQ power supply:</b> 1.35V, 1.283–1.45V operational; compatible to 1.5V operation.
$V_{REFCA}$	Supply	<b>Reference voltage for control, command, and address:</b> $V_{REFCA}$ must be maintained at all times (including self refresh) for proper device operation.
$V_{REFDQ}$	Supply	<b>Reference voltage for data:</b> $V_{REFDQ}$ must be maintained at all times (excluding self refresh) for proper device operation.
$V_{SS}$	Supply	Ground.
$V_{SSQ}$	Supply	<b>DQ ground:</b> Isolated on the device for improved noise immunity.
ZQ	Reference	<b>External reference ball for output drive calibration:</b> This ball is tied to an external 240 $\Omega$ resistor (RZQ), which is tied to $V_{SSQ}$ .
NC	–	<b>No connect:</b> These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).



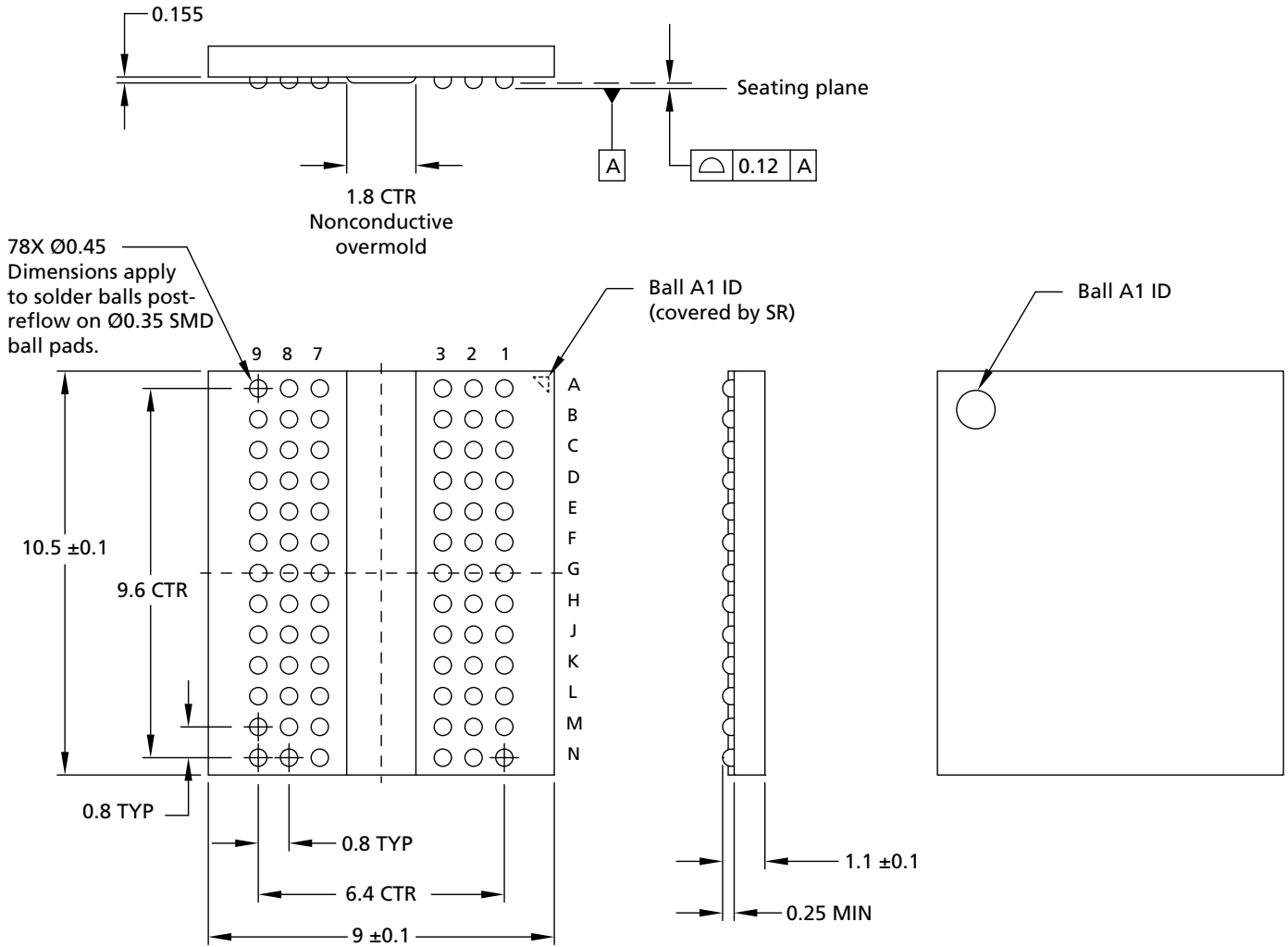
## Package Dimensions

Figure 4: 78-Ball FBGA – x4, x8 (RA)



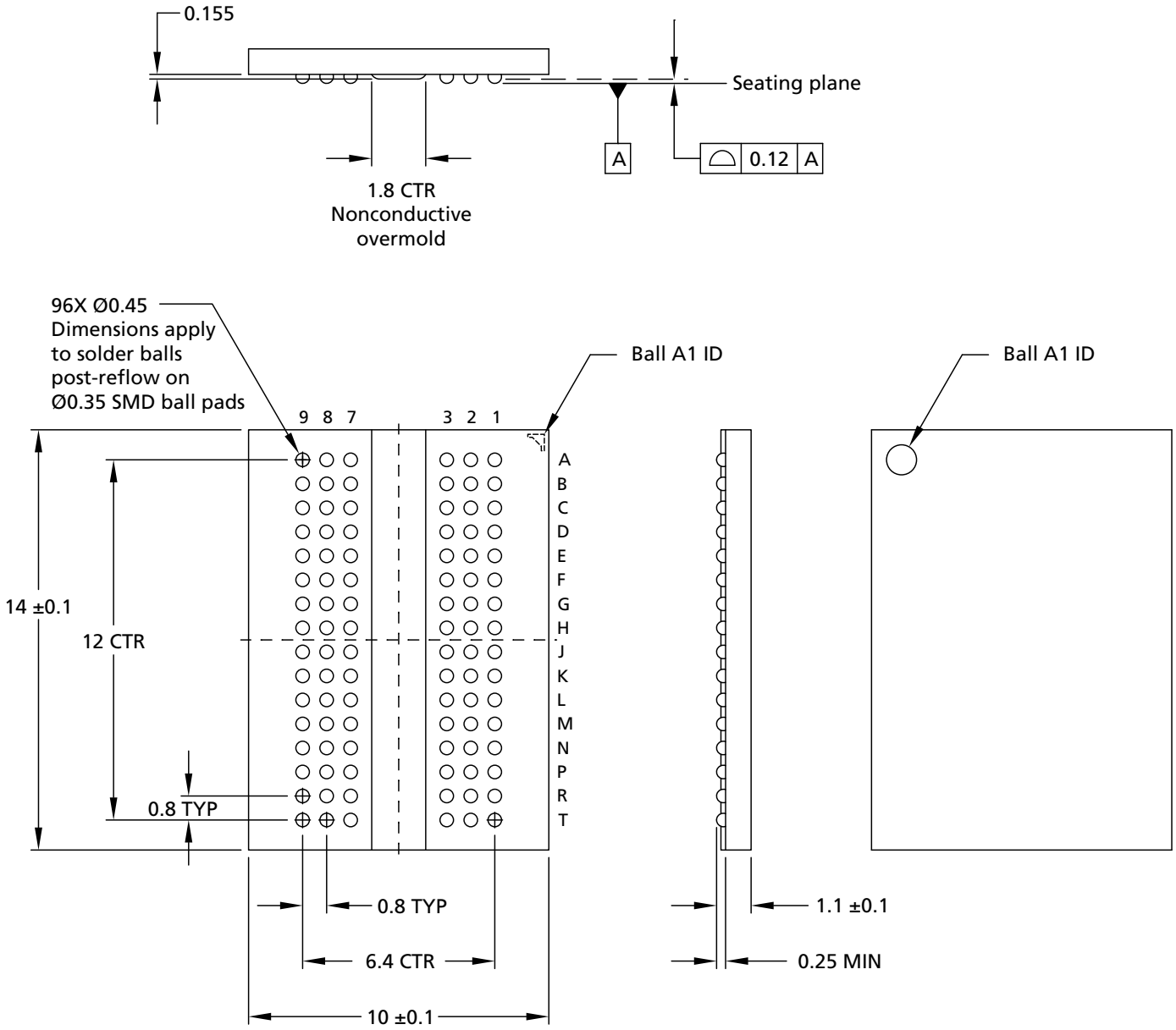
Note: 1. All dimensions are in millimeters.

**Figure 5: 78-Ball FBGA – x4, x8 (RH)**



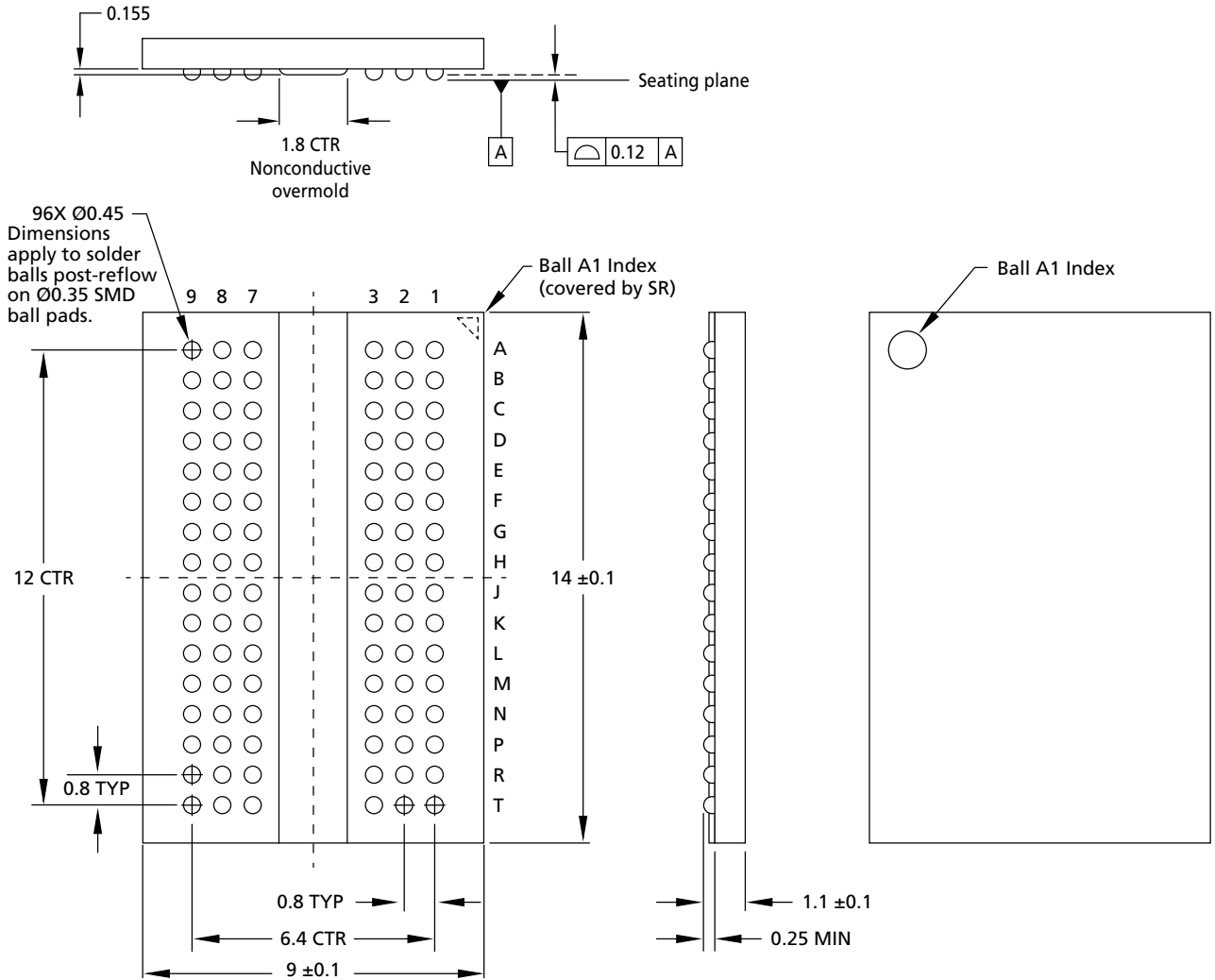
Note: 1. All dimensions are in millimeters.

**Figure 6: 96-Ball FBGA – x16 (RE)**



Note: 1. All dimensions are in millimeters.

**Figure 7: 96-Ball FBGA – x16 (HA)**



Note: 1. All dimensions are in millimeters.



## Electrical Characteristics – 1.35V operating I<sub>DD</sub> Specifications

**Table 5: I<sub>DD</sub> Maximum Limits - Die Rev. D**

Speed Bin			DDR3L-1066	DDR3L-1333	DDR3L-1600	Units
Parameter	Symbol	Width				
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I <sub>DD0</sub>	x4, x8	60	65	75	mA
		x16	75	80	90	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRE- CHARGE	I <sub>DD1</sub>	x4	70	75	80	mA
		x8	77	82	87	mA
		x16	105	110	115	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub>	All	20	20	20	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub>	All	30	32	37	mA
Precharge quiet standby current	I <sub>DD2Q</sub>	All	39	44	47	mA
Precharge standby current	I <sub>DD2N</sub>	All	42	45	50	mA
Precharge standby ODT current	I <sub>DD2NT</sub>	x4, x8	40	45	50	mA
		x16	45	50	55	mA
Active power-down current	I <sub>DD3P</sub>	All	53	58	63	mA
Active standby current	I <sub>DD3N</sub>	x4, x8	52	57	62	mA
		x16	68	73	77	mA
Burst read operating current	I <sub>DD4R</sub>	x4	135	155	175	mA
		x8	147	164	187	mA
		x16	220	240	280	mA
Burst write operating current	I <sub>DD4W</sub>	x4	115	135	155	mA
		x8	125	145	165	mA
		x16	180	200	225	mA
Burst refresh current	I <sub>DD5B</sub>	All	205	210	220	mA
Room temperature self refresh	I <sub>DD6</sub>	All	22	22	22	mA
Extended temperature self re- fresh	I <sub>DD6ET</sub>	All	28	28	28	mA
All banks interleaved read cur- rent	I <sub>DD7</sub>	x4, x8	210	250	290	mA
		x16	260	285	320	mA
Reset current	I <sub>DD8</sub>	All	I <sub>DD2P</sub> + 2mA	I <sub>DD2P</sub> + 2mA	I <sub>DD2P</sub> + 2mA	mA



**Table 6: I<sub>DD</sub> Maximum Limits Die Rev. E, J**

Speed Bin			DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Units
Parameter	Symbol	Width					
Operating current 0: One bank ACTIVATE-to-PRE-CHARGE	I <sub>DD0</sub>	x4, x8	44	47	55	62	mA
		x16	55	58	66	73	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I <sub>DD1</sub>	x4	53	57	61	65	mA
		x8	59	62	66	70	mA
		x16	80	84	87	91	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub>	All	18	18	18	18	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub>	All	26	28	32	37	mA
Precharge quiet standby current	I <sub>DD2Q</sub>	All	27	28	32	35	mA
Precharge standby current	I <sub>DD2N</sub>	All	28	29	32	35	mA
Precharge standby ODT current	I <sub>DD2NT</sub>	x4, x8	32	35	39	42	mA
		x16	35	39	42	45	mA
Active power-down current	I <sub>DD3P</sub>	All	32	35	38	41	mA
Active standby current	I <sub>DD3N</sub>	x4, x8	32	35	38	41	mA
		x16	41	45	47	49	mA
Burst read operating current	I <sub>DD4R</sub>	x4	113	130	147	164	mA
		x8	123	140	157	174	mA
		x16	185	202	235	252	mA
Burst write operating current	I <sub>DD4W</sub>	x4	87	103	118	133	mA
		x8	95	110	125	141	mA
		x16	137	152	171	190	mA
Burst refresh current	I <sub>DD5B</sub>	All	144	148	155	162	mA
Room temperature self refresh	I <sub>DD6</sub>	All	20	20	20	20	mA
Extended temperature self refresh	I <sub>DD6ET</sub>	All	25	25	25	25	mA
All banks interleaved read current	I <sub>DD7</sub>	x4, x8	160	190	220	251	mA
		x16	198	217	243	274	mA
Reset current	I <sub>DD8</sub>	All	I <sub>DD2P</sub> + 2mA	I <sub>DD2P</sub> + 2mA	I <sub>DD2P</sub> + 2mA	I <sub>DD2P</sub> + 2mA	mA

## Electrical Specifications

**Table 7: Input/Output Capacitance**

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Capacitance Parameters	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single-end I/O: DQ, DM	$C_{IO}$	1.5	2.5	1.5	2.5	1.5	2.3	1.5	2.2	1.5	2.1	pF
Differential I/O: DQS, DQS#, TDQS, TDQS#	$C_{IO}$	1.5	2.5	1.5	2.5	1.5	2.3	1.5	2.2	1.5	2.1	pF
Inputs (CTRL, CMD, ADDR)	$C_I$	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF

**Table 8: DC Electrical Characteristics and Operating Conditions – 1.35V Operation**

All voltages are referenced to  $V_{SS}$

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	$V_{DD}$	1.283	1.35	1.45	V	1, 2, 3, 4
I/O supply voltage	$V_{DDQ}$	1.283	1.35	1.45	V	1, 2, 3, 4

- Notes:
1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of  $V_{DD}/V_{DDQ}(t)$  over a very long period of time (for example, 1 sec).
  2. If the maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
  3. Under these supply voltages, the device operates to this DDR3L specification.
  4. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while  $V_{DD}$  and  $V_{DDQ}$  are changed for DDR3 operation (see Figure 8 (page 27)).

**Table 9: DC Electrical Characteristics and Operating Conditions – 1.5V Operation**

All voltages are referenced to  $V_{SS}$

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	$V_{DD}$	1.425	1.5	1.575	V	1, 2, 3
I/O supply voltage	$V_{DDQ}$	1.425	1.5	1.575	V	1, 2, 3

- Notes:
1. If the minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
  2. Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifications under the same speed timings as defined for this device.
  3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while  $V_{DD}$  and  $V_{DDQ}$  are changed for DDR3L operation (see Figure 8 (page 27)).

**Table 10: Input Switching Conditions – Command and Address**

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	DDR3L-1866	Units
Input high AC voltage: Logic 1	$V_{IH(AC160)min}^1$	160	160	–	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}^1$	135	135	135	mV
Input high AC voltage: Logic 1	$V_{IH(AC125)min}^1$	–	–	125	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC125)min}^1$	–	–	–125	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)min}^1$	–135	–135	–135	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)min}^1$	–160	–160	–	mV

Note: 1. When two  $V_{IH(AC)}$  values (and two corresponding  $V_{IL(AC)}$  values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one  $V_{IH(AC)}$  value may be used for address/command inputs and the other  $V_{IH(AC)}$  value may be used for data inputs.

For example, for DDR3L-800, two input AC levels are defined:  $V_{IH(AC160),min}$  and  $V_{IH(AC135),min}$  (corresponding  $V_{IL(AC160),min}$  and  $V_{IL(AC135),min}$ ). For DDR3L-800, the address/command inputs must use either  $V_{IH(AC160),min}$  with  $t_{IS(AC160)}$  of 215ps or  $V_{IH(AC135),min}$  with  $t_{IS(AC135)}$  of 365ps; independently, the data inputs may use either  $V_{IH(AC160),min}$  or  $V_{IH(AC135),min}$ .

**Table 11: Input Switching Conditions – DQ and DM**

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	DDR3L-1866	Units
Input high AC voltage: Logic 1	$V_{IH(AC160)min}^1$	160	160	–	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}^1$	135	135	135	mV
Input high AC voltage: Logic 1	$V_{IH(AC130)min}^1$	–	–	130	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC130)min}^1$	–	–	–130	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)min}^1$	–135	–135	–135	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)min}^1$	–160	–160	–	mV

Note: 1. When two  $V_{IH(AC)}$  values (and two corresponding  $V_{IL(AC)}$  values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one  $V_{IH(AC)}$  value may be used for address/command inputs and the other  $V_{IH(AC)}$  value may be used for data inputs.

For example, for DDR3L-800, two input AC levels are defined:  $V_{IH(AC160),min}$  and  $V_{IH(AC135),min}$  (corresponding  $V_{IL(AC160),min}$  and  $V_{IL(AC135),min}$ ). For DDR3L-800, the data inputs must use either  $V_{IH(AC160),min}$  with  $t_{IS(AC160)}$  of 90ps or  $V_{IH(AC135),min}$  with  $t_{IS(AC135)}$  of 140ps; independently, the address/command inputs may use either  $V_{IH(AC160),min}$  or  $V_{IH(AC135),min}$ .



**Table 12: Differential Input Operating Conditions (CK, CK# and DQS, DQS#)**

Parameter/Condition	Symbol	Min	Max	Units
Differential input logic high – slew	$V_{IH,diff(AC)slew}$	180	N/A	mV
Differential input logic low – slew	$V_{IL,diff(AC)slew}$	N/A	-180	mV
Differential input logic high	$V_{IH,diff(AC)}$	$2 \times (V_{IH(AC)} - V_{REF})$	$V_{DD}/V_{DDQ}$	mV
Differential input logic low	$V_{IL,diff(AC)}$	$V_{SS}/V_{SSQ}$	$2 \times (V_{IL(AC)} - V_{REF})$	mV
Single-ended high level for strobes	$V_{SEH}$	$V_{DDQ}/2 + 160$	$V_{DDQ}$	mV
Single-ended high level for CK, CK#		$V_{DD}/2 + 160$	$V_{DD}$	mV
Single-ended low level for strobes	$V_{SEL}$	$V_{SSQ}$	$V_{DDQ}/2 - 160$	mV
Single-ended low level for CK, CK#		$V_{SS}$	$V_{DD}/2 - 160$	mV

**Table 13: Minimum Required Time  $t_{DVAC}$  for CK/CK#, DQS/DQS# Differential for AC Ringback**

Slew Rate (V/ns)	DDR3L-800/1066/1333/1600		DDR3L-1866		
	$t_{DVAC}$ at 320mV (ps)	$t_{DVAC}$ at 270mV (ps)	$t_{DVAC}$ at 270mV (ps)	$t_{DVAC}$ at 250mV (ps)	$t_{DVAC}$ at 260mV (ps)
>4.0	189	201	163	168	176
4.0	189	201	163	168	176
3.0	162	179	140	147	154
2.0	109	134	95	105	111
1.8	91	119	80	91	97
1.6	69	100	62	74	78
1.4	40	76	37	52	55
1.2	Note1	44	5	22	24
1.0	Note1	Note1	Note1	Note1	Note1
<1.0	Note1	Note1	Note1	Note1	Note1

Note: 1. Rising input signal shall become equal to or greater than  $V_{IH(ac)}$  level and Falling input signal shall become equal to or less than  $V_{IL(ac)}$  level.

**Table 14: R<sub>TT</sub> Effective Impedance**

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [9, 6, 2]	R <sub>TT</sub>	Resistor	V <sub>OUT</sub>	Min	Nom	Max	Units
0, 1, 0	120Ω	R <sub>TT,120PD240</sub>	0.2 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/1
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/1
			0.8 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/1
		R <sub>TT,120PU240</sub>	0.2 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/1
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/1
			0.8 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/1
	120Ω		V <sub>IL(AC)</sub> to V <sub>IH(AC)</sub>	0.9	1.0	1.65	RZQ/2
0, 0, 1	60Ω	R <sub>TT,60PD120</sub>	0.2 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/2
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/2
			0.8 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/2
		R <sub>TT,60PU120</sub>	0.2 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/2
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/2
			0.8 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/2
	60Ω		V <sub>IL(AC)</sub> to V <sub>IH(AC)</sub>	0.9	1.0	1.65	RZQ/4
0, 1, 1	40Ω	R <sub>TT,40PD80</sub>	0.2 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/3
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/3
			0.8 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/3
		R <sub>TT,40PU80</sub>	0.2 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/3
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/3
			0.8 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/3
	40Ω		V <sub>IL(AC)</sub> to V <sub>IH(AC)</sub>	0.9	1.0	1.65	RZQ/6
1, 0, 1	30Ω	R <sub>TT,30PD60</sub>	0.2 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/4
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/4
			0.8 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/4
		R <sub>TT,30PU60</sub>	0.2 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/4
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/4
			0.8 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/4
	30Ω		V <sub>IL(AC)</sub> to V <sub>IH(AC)</sub>	0.9	1.0	1.65	RZQ/8
1, 0, 0	20Ω	R <sub>TT,20PD40</sub>	0.2 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/6
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/6
			0.8 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/6
		R <sub>TT,20PU40</sub>	0.2 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/6
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/6
			0.8 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/6
	20Ω		V <sub>IL(AC)</sub> to V <sub>IH(AC)</sub>	0.9	1.0	1.65	RZQ/12

**Table 15: Reference Settings for ODT Timing Measurements**

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Measured Parameter	R <sub>TT,nom</sub> Setting	R <sub>TT(WR)</sub> Setting	V <sub>SW1</sub>	V <sub>SW2</sub>
t <sub>AON</sub>	RZQ/4 (60Ω)	N/A	50mV	100mv
	RZQ/12 (20Ω)	N/A	100mV	200mV
t <sub>AOFF</sub>	RZQ/4 (60Ω)	N/A	50mV	100mv
	RZQ/12 (20Ω)	N/A	100mV	200mV
t <sub>AONPD</sub>	RZQ/4 (60Ω)	N/A	50mV	100mv
	RZQ/12 (20Ω)	N/A	100mV	200mV
t <sub>AOFPD</sub>	RZQ/4 (60Ω)	N/A	50mV	100mv
	RZQ/12 (20Ω)	N/A	100mV	200mV
t <sub>ADC</sub>	RZQ/12 (20Ω)	RZQ/2 (20Ω)	200mV	250mV

**Table 16: 34Ω Driver Impedance Characteristics**

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [5, 1]	R <sub>ON</sub>	Resistor	V <sub>OUT</sub>	Min	Nom	Max <sup>1</sup>	Units
0, 1	34.3Ω	R <sub>ON,34PD</sub>	0.2 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/7
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/7
			0.8 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/7
		R <sub>ON,34PU</sub>	0.2 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/7
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/7
			0.8 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/7
Pull-up/pull-down mismatch (MM <sub>PUPD</sub> )			V <sub>IL(AC)</sub> to V <sub>IH(AC)</sub>	-10	N/A	10	%

Note: 1. A larger maximum limit will result in slightly lower minimum currents.

**Table 17: 40Ω Driver Impedance Characteristics**

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [5, 1]	R <sub>ON</sub>	Resistor	V <sub>OUT</sub>	Min	Nom	Max <sup>1</sup>	Units
0, 0	40Ω	R <sub>ON,40PD</sub>	0.2 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/6
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/6
			0.8 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/6
		R <sub>ON,40PU</sub>	0.2 × V <sub>DDQ</sub>	0.9	1.0	1.45	RZQ/6
			0.5 × V <sub>DDQ</sub>	0.9	1.0	1.15	RZQ/6
			0.8 × V <sub>DDQ</sub>	0.6	1.0	1.15	RZQ/6
Pull-up/pull-down mismatch (MM <sub>PUPD</sub> )			V <sub>IL(AC)</sub> to V <sub>IH(AC)</sub>	-10	N/A	10	%

Note: 1. A larger maximum limit will result in slightly lower minimum currents.

**Table 18: Single-Ended Output Driver Characteristics**

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Parameter/Condition	Symbol	Min	Max	Units
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.09 \times V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.09 \times V_{DDQ}$	$SRQ_{se}$	1.75	6	V/ns

**Table 19: Differential Output Driver Characteristics**

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Parameter/Condition	Symbol	Min	Max	Units
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.18 \times V_{DDQ}$ and $V_{OH,diff(AC)} = 0.18 \times V_{DDQ}$	$SRQ_{diff}$	3.5	12	V/ns
Output differential crosspoint voltage	$V_{OX(AC)}$	$V_{REF} - 135$	$V_{REF} + 135$	mV

**Table 20: Electrical Characteristics and AC Operating Conditions**

Note 1 applies to base timing specifications

Parameter		Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>DQ Input Timing</b>													
Data setup time to DQS, DQS#	Base (specification)	$t_{DS}^{(AC160)}$	90	–	40	–	N/A	–	N/A	–	N/A	–	ps
	$V_{REF} @ 1 V/ns$		250	–	200	–	N/A	–	N/A	–	N/A	–	ps
Data setup time to DQS, DQS#	Base (specification)	$t_{DS}^{(AC135)}$	140	–	90	–	45	–	25	–	N/A	–	ps
	$V_{REF} @ 1 V/ns$		275	–	225	–	180	–	160	–	N/A	–	ps
Data hold time from DQS, DQS#	Base (specification)	$t_{DH}^{(DC90)}$	160	–	110	–	75	–	55	–	N/A	–	ps
	$V_{REF} @ 1 V/ns$		250	–	200	–	165	–	145	–	N/A	–	ps
Data setup time to DQS, DQS#	Base (specification)	$t_{DS}^{(AC130)}$	N/A	–	N/A	–	N/A	–	N/A	–	70	–	ps
	$V_{REF} @ 2 V/ns$		N/A	–	N/A	–	N/A	–	N/A	–	135	–	ps
Data hold time from DQS, DQS#	Base (specification)	$t_{DH}^{(DC90)}$	N/A	–	N/A	–	N/A	–	N/A	–	75	–	ps
	$V_{REF} @ 2 V/ns$		N/A	–	N/A	–	N/A	–	N/A	–	110	–	ps
<b>Command and Address Timing</b>													
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	$t_{IS}^{(AC160)}$	215	–	140	–	80	–	60	–	N/A	–	ps
	$V_{REF} @ 1 V/ns$		375	–	300	–	240	–	220	–	N/A	–	ps
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	$t_{IS}^{(AC135)}$	365	–	290	–	205	–	185	–	65	–	ps
	$V_{REF} @ 1 V/ns$		500	–	425	–	340	–	320	–	200	–	ps

**Table 20: Electrical Characteristics and AC Operating Conditions (Continued)**

Note 1 applies to base timing specifications

Parameter		Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	$t_{IS}^{(AC125)}$	N/A	–	N/A	–	N/A	–	N/A	–	150	–	ps
	$V_{REF} @ 1 V/ns$		N/A	–	N/A	–	N/A	–	N/A	–	275	–	ps
CTRL, CMD, ADDR hold from CK, CK#	Base (specification)	$t_{IH}^{(DC90)}$	285	–	210	–	150	–	130	–	110	–	ps
	$V_{REF} @ 1 V/ns$		375	–	300	–	240	–	220	–	200	–	ps

- Notes: 1. When two  $V_{IH(AC)}$  values (and two corresponding  $V_{IL(AC)}$  values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one  $V_{IH(AC)}$  value may be used for address/command inputs and the other  $V_{IH(AC)}$  value may be used for data inputs.

For example, for DDR3-800, two input AC levels are defined:  $V_{IH(AC160),min}$  and  $V_{IH(AC135),min}$  (corresponding  $V_{IL(AC160),min}$  and  $V_{IL(AC135),min}$ ). For DDR3-800, the address/command inputs must use either  $V_{IH(AC160),min}$  with  $t_{IS(AC160)}$  of 215ps or  $V_{IH(AC135),min}$  with  $t_{IS(AC135)}$  of 365ps; independently, the data inputs must use either  $V_{IH(AC160),min}$  with  $t_{DS(AC160)}$  of 90ps or  $V_{IH(AC135),min}$  with  $t_{DS(AC135)}$  of 140ps.

2. When DQ single-ended slew rate is 1V/ns, the DQS differential slew rate is 2V/ns; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns;

**Table 21: Derating Values for  $t_{IS}/t_{IH}$  – AC160/DC90-Based**

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$
2.0	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	–1	–3	–1	–3	–1	–3	7	5	15	13	23	21	31	31	39	47
0.8	–3	–8	–3	–8	–3	–8	5	1	13	9	21	17	29	27	37	43
0.7	–5	–13	–5	–13	–5	–13	3	–5	11	3	19	11	27	21	35	37
0.6	–8	–20	–8	–20	–8	–20	0	–12	8	–4	16	4	24	14	32	30
0.5	–20	–30	–20	–30	–20	–30	–12	–22	–4	–14	4	–6	12	4	20	20
0.4	–40	–45	–40	–45	–40	–45	–32	–37	–24	–29	–16	–21	–8	–11	0	5



Table 22: Derating Values for  $t_{IS}/t_{IH}$  – AC135/DC90-Based

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$
2.0	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	2	-3	2	-3	2	-3	10	5	18	13	26	21	34	31	42	47
0.8	3	-8	3	-8	3	-8	11	1	19	9	27	17	35	27	43	43
0.7	6	-13	6	-13	6	-13	14	-5	22	3	30	11	38	21	46	37
0.6	9	-20	9	-20	9	-20	17	-12	25	-4	33	4	41	14	49	30
0.5	5	-30	5	-30	5	-30	13	-22	21	-14	29	-6	37	4	45	20
0.4	-3	-45	-3	-45	-3	-45	6	-37	14	-29	22	-21	30	-11	38	5

Table 23: Derating Values for  $t_{IS}/t_{IH}$  – AC125/DC90-Based

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$
2.0	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	3	-3	3	-3	3	-3	11	5	19	13	27	21	35	31	43	47
0.8	6	-8	6	-8	6	-8	14	1	22	9	30	17	38	27	46	43
0.7	10	-13	10	-13	10	-13	18	-5	26	3	34	11	42	21	50	37
0.6	16	-20	16	-20	16	-20	24	-12	32	-4	40	4	48	14	56	30
0.5	15	-30	15	-30	15	-30	23	-22	31	-14	39	-6	47	4	55	20
0.4	13	-45	13	-45	13	-45	21	-37	29	-29	37	-21	45	-11	53	5



**Table 24: Minimum Required Time  $t_{VAC}$  Above  $V_{IH(AC)}$  (Below  $V_{IL(AC)}$ ) for Valid ADD/CMD Transition**

Slew Rate (V/ns)	DDR3L-800/1066/1333/1600		DDR3L-1866	
	$t_{VAC}$ at 160mV (ps)	$t_{VAC}$ at 135mV (ps)	$t_{VAC}$ at 135mV (ps)	$t_{VAC}$ at 125mV (ps)
>2.0	70	209	200	205
2.0	53	198	200	205
1.5	47	194	178	184
1.0	35	186	133	143
0.9	31	184	118	129
0.8	26	181	99	111
0.7	20	177	75	89
0.6	12	171	43	59
0.5	Note 1	164	Note 1	18
<0.5	Note 1	164	Note 1	18

Note: 1. Rising input signal shall become equal to or greater than  $V_{IH(AC)}$  level and Falling input signal shall become equal to or less than  $V_{IL(AC)}$  level.

**Table 25: Derating Values for  $t_{DS}/t_{DH}$  – AC160/DC90-Based**

$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$
2.0	80	45	80	45	80	45										
1.5	53	30	53	30	53	30	61	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			-1	-3	-1	-3	7	5	15	13	23	21				
0.8					-3	-8	5	1	13	9	21	17	29	27		
0.7							-3	-5	11	3	19	11	27	21	35	37
0.6									8	-4	16	4	24	14	32	30
0.5											4	6	12	4	20	20
0.4													-8	-11	0	5

**Table 26: Derating Values for  $t_{DS}/t_{DH}$  – AC135/DC90-Based**

$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$
2.0	68	45	68	45	68	45										
1.5	45	30	45	30	45	30	53	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			2	-3	2	-3	10	5	18	13	26	21				
0.8					3	-8	11	1	19	9	27	17	35	27		
0.7							14	-5	22	3	30	11	38	21	46	37
0.6									25	-4	33	4	41	14	49	30
0.5											39	-6	37	4	45	20
0.4													30	-11	38	5



**Table 27: Derating Values for  $t_{DS}^{\Delta}$ / $t_{DH}^{\Delta}$  – AC130/DC100-Based at 2V/ns**

Shaded cells indicate slew rate combinations not supported

<b><math>\Delta t_{DS}</math>, <math>\Delta t_{DH}</math> Derating (ps) – AC/DC-Based</b>																										
<b>DQ Slew Rate V/ns</b>		<b>DQS, DQS# Differential Slew Rate</b>																								
		<b>8.0 V/ns</b>		<b>7.0 V/ns</b>		<b>6.0 V/ns</b>		<b>5.0 V/ns</b>		<b>4.0 V/ns</b>		<b>3.0 V/ns</b>		<b>2.0 V/ns</b>		<b>1.8 V/ns</b>		<b>1.6 V/ns</b>		<b>1.4 V/ns</b>		<b>1.2 V/ns</b>		<b>1.0 V/ns</b>		
		$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	
4.0		33	23	33	23	33	23																			
3.5		28	19	28	19	28	19	28	19																	
3.0		22	15	22	15	22	15	22	15	22	15															
2.5				13	9	13	9	13	9	13	9	13	9													
2.0						0	0	0	0	0	0	0	0	0	0											
1.5								-22	-15	-22	-15	-22	-15	-22	-15	-14	-7									
1.0										-65	-45	-65	-45	-65	-45	-57	-37	-49	-29							
0.9												-62	-48	-62	-48	-54	-40	-46	-32	-38	-24					
0.8														-61	-53	-53	-45	-45	-37	-37	-29	-29	-19			
0.7																-49	-50	-41	-42	-33	-34	-25	-24	-17	-8	
0.6																		-37	-49	-29	-41	-21	-31	-13	-15	
0.5																				-31	-51	-23	-41	-15	-25	
0.4																						-28	-56	-20	-40	

**Table 28: Minimum Required Time  $t_{VAC}$  Above  $V_{IH(AC)}$  (Below  $V_{IL(AC)}$ ) for Valid DQ Transition**

Slew Rate (V/ns)	$t_{VAC}$ at 160mV (ps)	$t_{VAC}$ at 135mV (ps)	$t_{VAC}$ at 130mV (ps)
>2.0	165	113	95
2.0	165	113	95
1.5	138	90	73
1.0	85	45	30
0.9	67	30	16
0.8	45	11	Note1
0.7	16	Note1	–
0.6	Note1	Note1	–
0.5	Note1	Note1	–
<0.5	Note1	Note1	–

Note: 1. Rising input signal shall become equal to or greater than  $V_{IH(AC)}$  level and Falling input signal shall become equal to or less than  $V_{IL(AC)}$  level.

## Initialization

If the SDRAM is powered up and initialized for the 1.35V operating voltage range, voltage can be increased to the 1.5V operating range provided that:

- Just prior to increasing the 1.35V operating voltages, no further commands are issued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.5V operating voltages are stable prior to issuing new commands, other than NOPs or COMMAND INHIBITs.
- The DLL is reset and relocked after the 1.5V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed.  $t_{ZQinit}$  must be satisfied after the 1.5V operating voltages are stable and prior to any READ command.

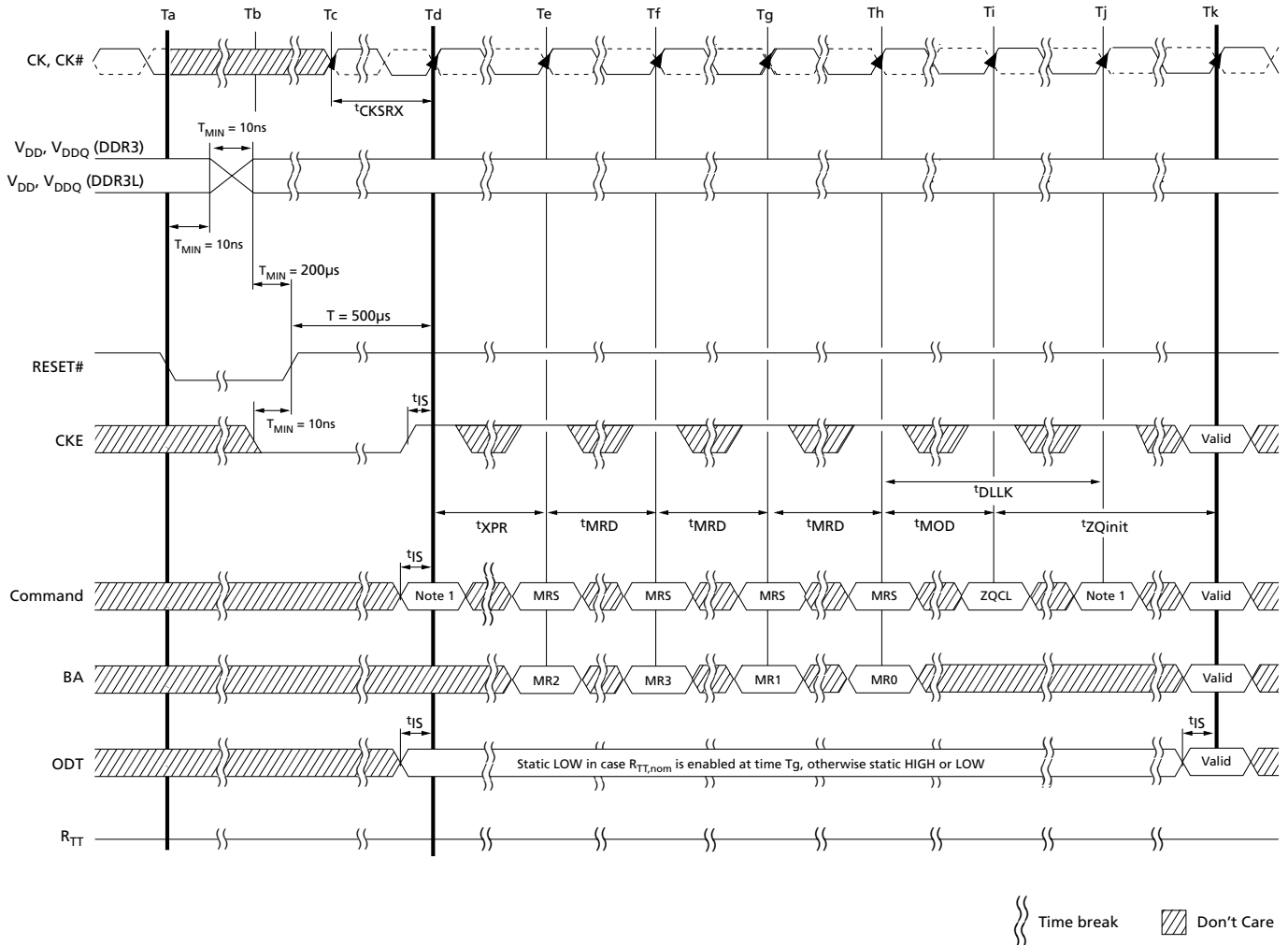
If the SDRAM is powered up and initialized for the 1.5V operating voltage range, voltage can be reduced to the 1.35V operation range provided that:

- Just prior to reducing the 1.5V operating voltages, no further commands are issued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.35V operating voltages are stable prior to issuing new commands, other than NOPs or COMMAND INHIBITs.
- The DLL is reset and relocked after the 1.35V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed.  $t_{ZQinit}$  must be satisfied after the 1.35V operating voltages are stable and prior to any READ command.

## V<sub>DD</sub> Voltage Switching

After the DDR3L DRAM is powered up and initialized, the power supply can be altered between the DDR3L and DDR3 levels, provided the sequence in Figure 8 is maintained.

**Figure 8: V<sub>DD</sub> Voltage Switching**



**Note:** 1. From time point Td until Tk, NOP or DES commands must be applied between MRS and ZQCL commands.

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